[0044] In some example embodiments of the present inventive concepts, the first portion of the first interlayer insulating layer may be an upper portion of the first interlayer insulating layer or a lower portion of the first interlayer insulating layer.

[0045] In some example embodiments of the present inventive concepts, the first portion of the first interlayer insulating layer may be an entirety of the first interlayer insulating layer.

[0046] In some example embodiments of the present inventive concepts, the oxidized element semiconductor material may include at least one of germanium (Ge) or silicon (Si).

[0047] In some example embodiments of the present inventive concepts, the semiconductor device may further include a third gate electrode on the substrate, a fourth gate electrode on the substrate, the fourth gate electrode adjacent to and spaced apart from the third gate electrode, a pair of third gate spacers at respective sides of the third gate electrode, a pair of fourth gate spacers at respective sides of the fourth gate electrode, a second interlayer insulating layer on the substrate, the second interlayer insulating layer between one of the pair of third gate spacers and one of the pair of fourth gate spacers opposing the one of the pair of third gate spacers.

[0048] In some example embodiments of the present inventive concepts, a first portion of the second interlayer insulating layer may include the oxidized element semiconductor material.

[0049] In some example embodiments of the present inventive concepts, an amount of the oxidized element semiconductor material included in the first portion of the first interlayer insulating layer may be different from an amount of the oxidized element semiconductor material included in the first portion of the second interlayer insulating layer.

[0050] In some example embodiments of the present inventive concepts, a thickness of the first portion of the first interlayer insulating layer may be different from a thickness of the first portion of the second interlayer insulating layer.

[0051] In some example embodiments of the present inventive concepts, the second interlayer insulating layer may not include the oxidized element semiconductor material.

[0052] In some example embodiments of the present inventive concepts, the second gate electrode and the third gate electrode may be a same electrode provided between the first gate electrode and the fourth gate electrode.

[0053] In some example embodiments of the present inventive concepts, slopes of the first, second, third, and fourth gate spacers or slopes of sidewalls of the first, second, third, and fourth gate electrodes may include both a positive sign and a negative sign.

BRIEF DESCRIPTION OF THE DRAWINGS

[0054] The above and other features and advantages of the present disclosure will become more apparent to those of ordinary skill in the art by describing in detail example embodiments thereof with reference to the accompanying drawings, in which:

[0055] FIG. **1** is a top view illustrating a semiconductor device according to an embodiment;

[0056] FIG. **2** is a cross-sectional view taken along line II-II' of FIG. **1**;

[0057] FIG. **3**A is a view illustrating a first gate spacer from which a first gate electrode of FIG. **2** is omitted;

[0058] FIG. **3**B illustrates the first gate electrode of FIG. **2** separately;

[0059] FIG. **4** schematically illustrates a concentration of an element semiconductor material along a scan line of FIG. **3**A;

[0060] FIGS. **5**A to **5**D are cross-sectional views taken along line V-V' of FIG. **1**;

[0061] FIGS. **6**A and **6**B are cross-sectional views illustrating a stress-relationship between an interlayer insulating layer and a gate spacer according to doping of an element semiconductor material;

[0062] FIG. **7** is a view illustrating a semiconductor device according to an example embodiment.

[0063] FIG. **8** is a view illustrating a semiconductor device according to an example embodiment;

[0064] FIG. **9** is a view illustrating a semiconductor device according to an example embodiment;

[0065] FIG. **10** is a view illustrating a semiconductor device according to an example embodiment;

[0066] FIG. **11** is a view illustrating a semiconductor device according to an example embodiment;

[0067] FIG. **12** is a view illustrating a semiconductor device according to an example embodiment;

[0068] FIG. **13** is a top view illustrating a semiconductor device according to an example embodiment;

[0069] FIG. **14** is a cross-sectional view taken along line XIV-XIV' of FIG. **13**;

[0070] FIG. **15** is a view illustrating a semiconductor device according to an example embodiment;

[0071] FIG. **16** is a top view illustrating a semiconductor device according to some example embodiments;

[0072] FIGS. **17**A and **17**B are cross-sectional views taken along lines XVII-A-XVII-A' and XVII-D-XVII-D' of FIG. **16**, according to an example embodiment;

[0073] FIGS. **18**A and **18**B are cross-sectional views taken along lines XVII-A-XVII-A' and XVII-D-XVII-D' of FIG. **16**, according to an example embodiment;

[0074] FIGS. **19**A and **19**B are cross-sectional views taken along lines XVII-A-XVII-A' and XVII-D-XVII-D' of FIG. **16**, according to an example embodiment;

[0075] FIGS. **20**A and **20**B are cross-sectional views taken along lines XVII-A-XVII-A' and XVII-D-XVII-D' of FIG. **16**, according to an example embodiment;

[0076] FIG. **21** is a view schematically illustrating a concentration profile of an element semiconductor material within a first interlayer insulating layer and a second interlayer insulating layer;

[0077] FIGS. **22**A and **22**B are cross-sectional views illustrating a semiconductor device taken along lines XVII-A-XVII-A' and XVII-D-XVII-D' of FIG. **16**, according to an example embodiment;

[0078] FIG. **23** is a view illustrating a semiconductor device according to an example embodiment;

[0079] FIG. **24**A is a top view of a fin-type pattern surrounded by field insulating layers, according an example embodiment. FIG. **24**B is a cross-sectional view taken on line—XXIV-XXIV' of FIG. **24**A;

[0080] FIGS. **25** to **31** are views illustrating a method of fabricating a semiconductor device according to an example embodiment; and